WE CLAIM

1. A method of modeling an integrated circuit, said method comprising the steps of:

(i) generating a circuit component model including signal transitions with a set of associated delays and rules for a given implementation of said integrated circuit;

(ii) calculating signal delays for signal transitions within said circuit component model using a delay calculator and a subset of said set of associated delays and rules; and

(iii) searching said circuit component model to identify signal transitions corresponding to signal transitions with associated signal delays as calculated by said delay calculator; and

(iv) modifying said circuit component model for identified matching signal transitions with said delays calculated by said delay calculator and said set of associated delays and rules.

2. A method as claimed in claim 1, wherein if said searching does not identify a matching signal relationship within said circuit component model for a signal transition and delay calculated by said delay calculator, then said signal transition and delay is passed directly to said circuit component model.

3. A method as claimed in claim 1, wherein said integrated circuit includes a macrocell which is modeled within said circuit component model other than by a details of individual circuit components.

4. A method as claimed in claim 3, wherein said macrocell is a microprocessor core.

5. A method as claimed in claim 1, wherein, if said circuit component model includes a plurality of a signal transitions that match a signal transition and delay calculated by said delay calculator, then said signal transition and delay calculated by

said delay calculator is used to modify all of said plurality of signal transitions within said circuit component model.

6. A method as claimed in claim 1, wherein if said signal transitions and delays calculated by said delay calculator include a plurality of signal transitions and delays that match a signal transition within said circuit component model, then that signal transition and delay calculated by said delay calculator that most specifically matches said signal transition within said circuit component model is used to modify said signal transition within said circuit component model.

7. A method as claimed in claim 1, wherein if signal transitions and delays calculated by said delay calculator include a signal transition and delay that is more specifically defined than any signal transition within said circuit component model, then the most specifically matching signal transition within said circuit component model is modified with said signal transition and delay.

8. A method as claimed in claim 1, further comprising the step of generating an audit log representing the steps taken.

9. A method as claimed in claim 7, further comprising the step of generating an audit log representing the steps taken and wherein said modification of said most specifically matching signal transition within said circuit component model with said more specifically defined signal transition and delay is recorded in said audit log.

10. A method as claimed in claim 1, wherein said set of associated delays and rules within said circuit component model includes associated condition parameters and said signal transitions and delays calculated by said delay calculator do not include condition parameters.

11. A method as claimed in claim 9, wherein different condition parameters of a signal transition within said circuit component model have different delays associated with them and said delay calculator calculates a delay for only one condition parameter.

12. A method as claimed in claim 10, wherein modified delay values for all of said condition parameters are inferred from said calculated delay using relative differences between said delays within said circuit component model.

13. A method as claimed in claim 1, wherein said associated set of delays and rules may include edge direction parameters.

14. A method as claimed claim 1, wherein said delay calculator outputs results as a standard delay format file.

15. A method as claimed in claim 1, wherein said circuit component model is a netlist model with associated timing and rule data.

16. A method as claimed in claim 15, wherein said associated timing and rule data is a standard delay format file.

17. A method as claimed in claim 16, wherein said step of modifying modifies said standard delay format file.

18. A method as claimed in claim 1, wherein said step of modifying is responsive to constraint data specifying instructions for how said modification should be performed.

19. Apparatus for modeling an integrated circuit, said apparatus comprising:

(i) a memory storing a circuit component model including signal transitions with a set of associated delays and rules for a given implementation of said integrated circuit;

(ii) a delay calculator for calculating signal delays for signal transitions within said circuit component model using a subset of said set of associated delays and rules; and

(iii) search logic for searching said circuit component model to identify signal transitions corresponding to signal transitions with associated signal delays as calculated by said delay calculator; and

(iv) modifying logic for modifying said circuit component model for identified matching signal transitions with said delays calculated by said delay calculator and said set of associated delays and rules.